Failure Analysis of Wafer using Backside OBIC Method

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Abstract

As a result of performing the Iddq (IC's power supply current) failure analysis on CMOS logic LSI using the backside OBIC (optical beam induced current) method, we succeeded in detecting a short circuit at an overlapped portion between a power supply line and a signal line. So far a circuit failure beneath the Al wiring has been difficult to find because the surface of LSI chip is covered by the wiring. However, we succeeded in detecting the carriers abnormally generated at a failure portion of a circuit on the chip surface by the optical energy when the backside of wafer was irradiated by an He-Ne laser. The backside OBIC technique is an effective method of failure analysis for advanced multilayer LSIs.

1. Introduction

The backside OBIC method is a technique to detect the carriers (electron-hole pair) generated by laser energy as current flowed out the interested current when laser light penetrated to silicon substrate. Until now, a failure portion has been detected by irradiating the front surface of sample chip by a laser, using the OBIC analyzer. [1,2] However, as the high density and multilayer Al wiring technology of LSI chip advance, a failure portion under the wiring becomes difficult to analyze from the front surface of the chip. [3]

Therefore, we proved experimentally that failure analysis can be done by detecting the current variation caused by the carrier generation, when the back side of a wafer by an He-Ne 1152 nm laser

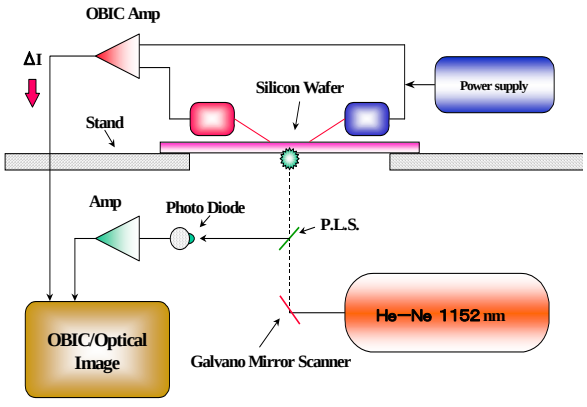

Fig. 1. Outline diagram of the backside OBIC imaging system

(hereafter referred to as IR laser) is irradiated. In this paper, we describe the effectiveness of the backside OBIC method and the results of failure analysis using this method.

2. Theory and backside OBIC system

To observe the front surface circuit pattern from the back side of a silicon wafer, a low energy laser which penetrates the silicon substrate is necessary. For example, considering the band-gap of silicon substrate of 1.107 eV (at 273 K), the He-Ne 1152 nm laser (1.076 eV) penetrates the silicon substrate, because no transition between the valence band and the conduction band occurs.[4] That is, the fact that the laser radiation from the back side of chip penetrates the silicon substrate, enables to view the surface circuit pattern from the back side of wafer.

If impurities are doped into the silicon substrate, the transition energy necessary to the band-gap of substrate becomes smaller than that of the intrinsic semiconductor. For example, the transition energy necessary when boron is doped into the silicon substrate decreases from 1.107 eV to 1.063 eV.

That is, with the IR laser used this time, it becomes difficult to penetrate the region where impurities were doped. On the other hand, it is easy to generate the carriers in the depletion layer. A technique to detect these carriers outside of the test circuit as a current variation is the OBIC method. The wavelength of the IR laser used this time is the optimum for penetrating the silicon substrate and generating the carriers in the surface circuit region.

The outline diagram of the backside OBIC system (JEOL JBS-1181) is shown in Fig. 1. The sample wafer was fixed at four peripheral portions by a vacuum chuck. The OBIC analysis image was created by converting the OBIC current into graphic signal. The OBIC current data was obtained by 2 dimensional scanning of IR laser irradiated the wafer backside. Out put power of IR laser is 2 mW, and scanning is made by a galvano mirror. The number of pixels was 512 x 512 pixels and it took one second to scan each graphic screen. The optical image of the circuit pattern viewed from the wafer front surface was obtained in the same manner as mentioned above, by laser scanning, receiving its reflected laser by an optical diode, and converted into a graphical image. The failure portion can be identified by overlaied the optical image with the OBIC image.

The voltage applied to the sample is supplied from the upper side of the wafer by probing. The detecting sensitivity of the OBIC amplifier is 40 pA and the maximum sink current is 20 mA.

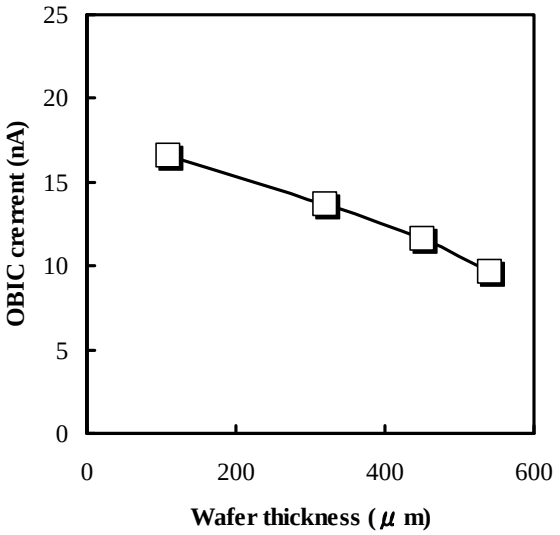

Fig. 2. Characteristics of OBIC current and wafer thickness. In the measurement, by applying reverse bias current to the p-n junction region of 10 μm × 30 μm, we measured the OBIC current flowing when an He-Ne laser of 1152 nm was irradiated from the back side of wafer.

3. Result of failure analysis

To perform the backside OBIC analysis, no special surface grinding for the back surface of wafer sample is necessary. This is because the depth of focus becomes shallow as the magnification of lens becomes higher and irregularity on the back surface of wafer can be ignored.

Fig. 2 is the graph showing the relationship between the OBIC current of the p-n junction and wafer thickness when the laser is irradiated from the back side of the wafer. Though the absolute value of the OBIC current decreases as the thickness of wafer becomes larger, the analytical image can be improved by increasing the gain of the OBIC amplifier. Considering the roughness of the back surface of the silicon wafer after the BG (back grind) process, the OBIC analysis can be performed up to the thickness of 500 μm. No special processing for wafer sample is required to perform the backside OBIC analysis.

A manufactured logic LSI's Iddq failure sample was analyzed by the backside OBIC method, using the CMOS 0.35 μm Al 3 layer wiring process.

The sample was analyzed by applying 3.3 V between a power supply line and GND using an LSI tester. It was found that a current of approximately 30 μA was flowing, which was an abnormal value compared with the normal current value of 1 μA. Considering that the circuit operation of the wafer sample was operating normally, there was a possibility of a high impedance short circuit between the power supply and the GND.

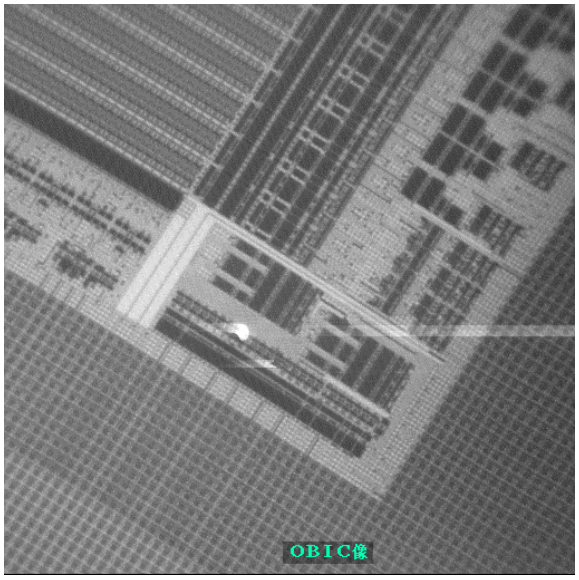

Fig. 3. Backside OBIC image 1800 magnification

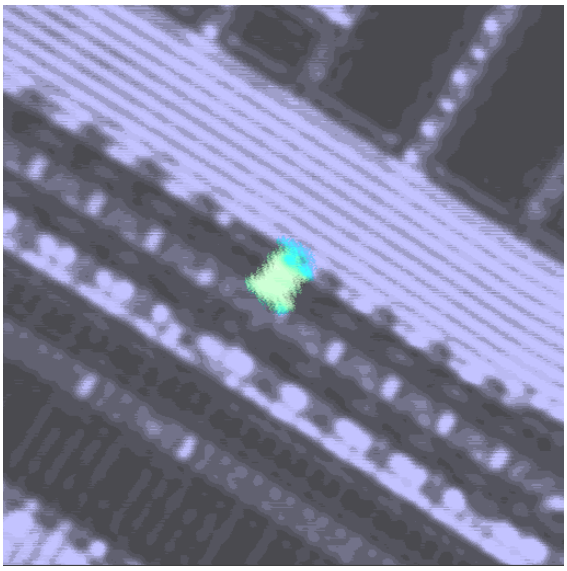

Fig. 4. Backside OBIC image 3600 magnification

The sample wafer was analyzed using the backside OBIC system and a bright spot likely to be a weak point was found in the random circuit. The OBIC current variation of the failure portion was approximately 1 μA. A bright spot was observed when a voltage of 0.1V to 0.3 V was applied between the power supply line and the GND. These results are shown in Fig. 3 & 4.

As a result of the detailed SEM investigation of the wafer sample, we found that the bright spot was not abnormal and there was parasitic resistance of approximately 100 KΩ which shunts between the inverter gate output and the power supply line. Fig. 5 shows SEM image in the Al wiring circuit short.

A strong OBIC current flows due to the reason that the bright spot of the analytical image has a higher electric field of depletion layer than other normal regions, which so far has been considered as a failure. Fig. 6 shows the equivalent circuit and cross-sectional diagram.

As the voltage for measurement used in the backside OBIC method, a fine analytical image could be obtained when the voltage is low. This is because the abnormal portion can be detected emphatically by suppressing the carrier generation at the normal portion.

Fig. 5. SEM image of Al wiring short.

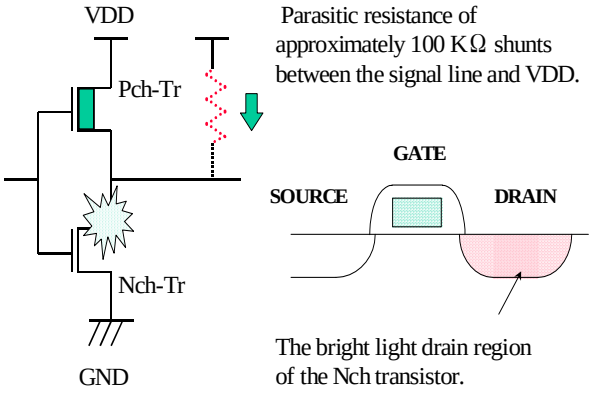

Fig. 6. CMOS circuit of the breakdown region, and cross section of the bright spot.

4. Conclusion

Until now, failure analysis of multilayer wiring LSIs has been difficult because the laser was intercepted by the surface Al wiring. However, we succeeded in detecting the photo-current of less than 1 μ A caused by carriers generated at a failure portion of the chip's surface circuit, by irradiating the back side of wafer sample with an He-Ne laser, using the backside OBIC method.

By applying a low voltage of 0.1 V to 0.3 V to the wafer sample, the carrier generation at normal portion is suppressed and the carrier generation (1 μ A equivalent) at the failure portion can be detected emphatically.

The silicon wafer used for the backside OBIC analysis can be analyzed despite its back surface roughness after BG process. Therefore, we don't have to prepare particularly. This is because the depth of lens focus becomes shallow and the ignored.

The wavelength of the He-Ne laser used this time is 1152 nm, which can penetrate the silicon substrate and generate the carriers in the surface circuit region. Therefore, we consider this wavelength as the optimum for the backside OBIC analysis.

Reference

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